IN THE SPECIFICATION

Please insert before the first paragraph under BACKGROUND OF THE INVENTION of page 1 of the disclosure currently on file with the following paragraph:

This application is a Divisional of nonprovisional application serial number 09/824,225 filed April 3, 2001. Priority is claimed based on U.S. Application No. 009/824,225 filed April 3, 2001, which claims the priority of Japanese application 2000-159544 filed on May 25, 2000.

Please replace page 5, last paragraph of the Disclosure currently on file with the following paragraph:

Then, a gate insulation film 155, a gate electrode 156, and a gate side wall insulation film 157 are formed to pMODFET, and a gate insulation film 158, a gate electrode 159, and a gate side wall insulation film 160 are formed to nMOSFET (refer to FIG. 50(~~d~~a)). Finally, p-type dopant is selectively ion implanted to form a source 161 and a drain 162 of pMODFET, and n-type dopant is selectively ion implanted to form a source 163 and a drain 164 of nMOSFET (refer to FIG. 50(eb)).

Please replace page 6, first paragraph of the Disclosure currently on file with the following paragraph:

Further, the result of study on the process flow in a case using a field insulation film and a device isolation insulation region is shown in FIG. 51 and FIG. 52. A field insulation film 165 in a region other than the region forming an intrinsic region for nMOSFET and pMODFET is formed on a silicon substrate 150, and a device isolation insulation film 166 is formed for isolation of the transistors (refer to FIG. 51(a)). Then, p-type and n-type dopants are ion implanted to the regions for forming nMOSFET and pMODFET, to form a p-well 151 and an n-well 152 respectively (refer to FIG. 51(b)). Then, a buffer layer 153 and a multi-layered film 154 comprising single-crystal silicon and single-crystal silicon-germanium are formed on the entire surface of the substrate by epitaxial growth. In this process, a multi-layered film of a single crystal silicon-germanium layer and a single-crystal silicon layer is formed on the silicon substrate, and a multi-layered film of a polycrystalline

silicon-germanium layer and a polycrystalline silicon layer are formed on the field insulation film 165 and the device isolation insulation film 166 (refer to FIG. 51(c)). In the region forming nMOSFET, since the surface of the silicon substrate 150 has to be exposed, the multi-layered film 154 comprising silicon and silicon-germanium and the buffer layer 153 are removed while leaving the region forming pMODFET (refer to FIG. 52(a~~d~~)). After forming a gate insulation film 155, a gate electrode 156 and a gate side wall insulation film 157 to pMODFET, and forming a gate insulation film 158, a gate electrode 159 and a gate side wall insulation film 160 to nMOSFET, p-type dopant is selectively ion implanted to form a source 161 and a drain 162 of pMODFET, and n-dopant is selectively ion implanted to form a source 163 and a drain 164 of nMOSFET (refer to FIG. 52(be)). As the result, the step between pMODFET and nMOSFET corresponds substantially to the thickness of the buffer layer 153 and the multi-layered film 154 comprising silicon and silicon-germanium.

At page 9, line 25, please insert the following paragraph:

FIG. 3 is an enlarged cross sectional view illustrating the steps after FIG. 2 successively.

At page 14, line 14, please delete the paragraph beginning with "A method of manufacturing the semiconductor device of the structure shown in Fig. 1...", and insert therefor:

A method of manufacturing the semiconductor device of the structure shown in Fig. 1 is explained with reference to Fig. 2.

Please replace page 15, third paragraph of the Disclosure currently on file with the following paragraph:

Then, a buffer layer 8, comprising single-crystal silicon-germanium, is formed by selective epitaxial growth on the silicon substrate 1 exposed at the bottom of the opening (refer to Fig. 3(a)~~2(d)~~). In the buffer layer 8, germanium content is increased from the silicon substrate 1 to the surface. A virtual substrate having favorable crystallinity at the surface and a lattice constant with a value of the single-crystal silicon-germanium layer is formed by relaxing strain due to the difference of the lattice constant between the single-crystal silicon and single-crystal silicon-germanium layer only in the inside of the buffer layer 8. For example, when the

germanium content is increased uniformly from 5% on the side of the silicon substrate 1 to 30% on the side of the surface, a crystal plane in which the strain is completely relaxed in the inside is obtained at the thickness of the buffer layer 8 of about 1.5 μm. Further, when the germanium content is increased not uniformly, but stepwise, the thickness of the buffer layer 8 can be reduced to obtain a satisfactory crystal surface with a thickness of about 1.0 μm.

Please replace page 19, third paragraph of the Disclosure currently on file with the following paragraph:

Then, a multi-layered film 9 comprising single-crystal silicon and single-crystal silicon-germanium is formed on the buffer layer 8 by selective epitaxial growth in the same manner as the method of forming the buffer layer 8 (refer to Fig. 3(b) ~~2(e)~~). Fig. 5 shows an enlarged view of an intrinsic region in pMODFET. At first, a carrier supply layer 9a containing a p-type dopant is formed by selective epitaxial growth on the buffer layer 8. In the carrier supply layer 9a, the germanium content may be made equal with the value on the side of the surface of the buffer layer, and the concentration of the dopant may be $1x10^{20}$cm-3 or less in order to suppress the diffusion to the channel layer. The thickness is suitable at 1 nm or more where the controllability for the epitaxial growth is preferred. A spacer layer 9b comprising single-crystal silicon-germanium as a barrier layer for confining carriers is formed. In the spacer layer, the germanium content may be made equal with a value on the side of the surface of the buffer layer 8, and the thickness may be within a range from 1 nm where the controllability for epitaxial growth is favorable to 50 nm where carriers are supplied to the channel layer. The channel layer 9c is put to a state undergoing compressive strain by making the germanium content higher than the spacer layer 9b. For example, the channel layer undergoes the compressive strain by defining the germanium content of the channel layer to 50% relative to the germanium content of 30% in the spacer layer 9b, and the valence band changes. As a result, the energy to the holes of the valence band in the channel layer is lowered to form a quantum well structure, so that carriers supplied from the carrier supply layer 9a are stored in the well layer to form two-dimensional hole gases. The thickness of the channel layer may be 1 nm or more where the controllability for epitaxial growth is favorable. A cap layer 9d forming a barrier layer for the carriers and comprising single-crystal silicon for protecting the silicon-germanium layer is formed on the

channel layer. The thickness for the cap layer is suitably from 1 nm, where the controllability for epitaxial growth is favorable, to 50 nm at which carrier can be controlled in the channel layer for the control from the gate electrode. In the embodiment shown in Fig. 5, the carrier supply layer 9a is present between the channel layer 9c and the buffer layer 8, but the carrier supply layer 9a may be on the side of the upper surface relative to the channel layer 9c. Fig. 6 shows an enlarged view for an intrinsic region for a pMODFET of this case. The spacer layer 9b, the channel layer 9c, the second spacer layer 9e, the carrier supply layer 9a and the cap layer 9d may be grown successively from the side of the buffer layer 8.

Please replace page 20, second paragraph of the Disclosure currently on file with the following paragraph:

After forming the multi-layered film 9 comprising single-crystal silicon and single-crystal silicon-germanium by selective epitaxial growth to the intrinsic region for the pMODFET, the gate insulation film 10 and the gate electrode 11 are deposited over the entire surface, the gate and the electrode 11 are anisotropically etched to form gate - source and gate - drain isolation insulation film 12 to the side wall of the gate electrode (refer to Fig. 3(c~~f~~)).

Please replace page 27, third paragraph to page 28, second paragraph of the Disclosure currently on file with the following three paragraphs:

Then, after depositing a first insulation film 23 and a second insulation film 24 over the entire surface, a high concentration p-type polycrystalline silicon 25 as a base lead electrode of the HBT and source--drain lead electrodes of the pMODFET are formed selectively (refer to FIG. 16(a~~d~~)).

An insulation film 26 is formed over the entire surface so as to cover the high concentration p-type polycrystalline silicon 25, and openings 27 are formed to the insulation film 26 and the high concentration p-type polycrystalline silicon 25 in the emitter portion of the HBT and the gate portion of the pMODFET. An insulation film 28 is formed to the side wall for each opening 27, and two layers of the insulation films 24 and 23 are etched by isotropic etching to form an overhang of the high concentration polycrystalline silicon layer 25 (refer to FIG. 16(b~~e~~)).

A multi-layered film 29 comprising single-crystal silicon and single-crystal silicon-germanium is epitaxially grown selectively to the opening 27 to form an

intrinsic base layer 29b in the region of the HBT, while a carrier supply layer and a channel layer are formed in the region of the pMODFET and, simultaneously, the polycrystalline silicon and polycrystalline silicon-germanium grown from below the overhang of the high concentration p-type polycrystalline silicon layer 25 are grown to automatically join the high concentration p-type polycrystalline silicon layer 25 and the multi-layered film 29 comprising the single-crystal silicon and single-crystal silicon-germanium automatically (refer to FIG. 16(cf)).

Please replace page 29, second & third paragraphs of the Disclosure currently on file with the following two paragraph:

After covering the surface of the multi-layered film 29 comprising single-crystal silicon and the single-crystal silicon-germanium layer with an insulation film 31, an insulation film 32 is formed selectively to the side wall of the opening. The insulation film 31 is etched in the opening of the HBT for forming an emitter region, but the insulation film 31 is used as the gate insulation film in the opening of the pMODFET (refer to FIG. 17(ag)).

A high concentration n-type single-crystal silicon 33 as an emitter and a gate electrode is formed to the opening, and an n-type dopant is diffused from the high concentration n-type polycrystalline silicon 33 into the multi-layered film 29 comprising the single-crystal silicon and single-crystal silicon-germanium layer only in the region of the HBT, for example, by annealing at 900 degrees C for 30 sec, to form an emitter region 34 (refer to FIG. 17(bh)).

Please replace page 33, second paragraph to page 35, first paragraph of the Disclosure currently on file with the following four paragraphs:

Then, insulation films 39 and 40 as a mask material for selective growth in the pMODFET are deposited over the entire surface, and an opening 27a is formed to the insulation films 40, 39 and 26, the high concentration polycrystalline silicon layer 25 and the insulation film 24 in the region of the pMODFET. Preferably, the insulation film 39 is made of a silicon oxide film and the insulation film 40 is made of a silicon nitride film. Then, insulation films 41 and 42 are further formed to the side wall of the opening (refer to FIG. 23(ae)). Preferably, the insulation film 41 is made of silicon oxide film, and the insulation film 42 is made of a silicon nitride film. Since all the portions other than the bottom of the opening 27a are covered with the silicon nitride

film in this step, the insulation film 23 and the field insulation film 2 are opened to expose the surface of the silicon substrate 1 (refer to FIG. 23(bf)).

Since the single-crystal silicon layer is exposed only at the bottom of the opening 27a, a buffer layer 43 of the pMODFET comprising single-crystal silicon-germanium is formed by selective epitaxial growth. When a silicon nitride film is formed on the side wall of the opening for suppressing occurrence of facets like that in the Embodiment 1, since the silicon nitride film is deposited also to the side wall of the source-drain lead electrode 25, the silicon nitride film has to be removed after epitaxial growth of the buffer layer in order to connect the source and the drain. However, when the silicon nitride film is removed, damages are caused to the surface of the buffer layer 43 comprising single-crystal silicon-germanium to greatly deteriorate the performance of the pMODFET formed on the surface thereof Accordingly, a method of suppressing the generation of the facets without using the silicon nitride film on the side wall is adopted. FIG. 26 and FIG. 27 show a relation between the shape of a single crystal layer 67 epitaxially grown in the opening of a silicon oxide film formed on the silicon substrate 61 and the crystal orientation of the opening. As shown in FIG. 26(a), when the opening is formed with the side being directed to [110] orientation in the in-plane crystal orientation of the silicon substrate 61, reconstruction of surface atoms occurs at the boundary between the silicon oxide film 66 and the silicon substrate 65, and on the surface of the single crystal layer 67, (111) and (311) planes having more stable surface state than (100) as the in-plane orientation of the substrate are formed. As a result, assuming that an ideal rectangular opening is formed, facets 63, 64 are formed from each side of the opening. As shown in FIG. 27, on the other hand, when the side of the opening is directed to [100] orientation, since rearrangement of the surface atom less occurs, the facet is not generated at each side, but small facet planes 63 and 64 are generated only at the corners of the opening. Accordingly, in most regions in the opening, the single crystal layer 67 grows so as to be in contact with the silicon oxide film 66. Utilizing this characteristic, even in a case of using a silicon oxide film as the field insulation film 2, the buffer layer 43 grows in contact with the field insulation film 2 in the opening by directing the side of the opening to [100] orientation to greatly reduce the effect of facets (refer to FIG. 23(cg)).

The insulation film 39 as the mask material for the selective growth is removed only in the region of the pMODFET, and the multi-layered film 44

comprising single-crystal silicon and single-crystal silicon-germanium and polycrystalline silicon and polycrystalline silicon-germanium simultaneously are formed, to the source-drain lead electrodes 25a and 25b and a channel layer in a self-aligned manner (refer to FIG. 24(a~~h~~)). The structure of the multi-layered film 44 comprising single-crystal silicon and single-crystal silicon-germanium is substantially identical with that in the Embodiment 1.

After depositing a gate insulation film 46 and forming an insulation film 47 on the side wall of the opening, insulation films 39 and 46 covering the bottom of the opening are removed only in the HBT region to expose the single-crystal silicon cap layer (refer to FIG. 24(b~~i~~)).

When high concentration n-type polycrystalline silicon layer is deposited only to the periphery of the openings of the HBT and the pMODFET and annealing is applied, the n-type dopant is diffused only in the HBT region to form an emitter region 34 (refer to FIG. 24(c~~j~~)). Removal of the overlap portion is substantially identical with that in the Embodiment 5.

Please replace page 36, last paragraph to page 37, third paragraph of the Disclosure currently on file with the following three paragraphs:

Then, an insulation film 39 as a mask for selective growth in the pMODFET is deposited over the entire surface, and an opening 27a for the insulation films 39, 26, 24 and 23 is formed in the region of the pMODFET. Since the buffer layer 21 as the single crystal layer is exposed to the bottom of the opening, a multi-layered film 9 comprising single-crystal silicon and single-crystal silicon-germanium is selectively grown epitaxially (refer to FIG. 30(a~~e~~)). In this case, the structure of the multi-layered film 9 comprising single-crystal silicon and single-crystal silicon-germanium is substantially identical with that in the Embodiment 1.

After depositing a gate insulation film 50 and a gate 51, and fabricating the gate 51, an insulation film 47 is formed to the opening of the HBT and the side wall of the gate of the pMODFET (refer to FIG. 30(b~~f~~)).

The insulation films 50 and 39 are removed by isotropic etching to expose the single-crystal silicon cap at the bottom of the opening in the HBT, and an emitter electrode comprising a high concentration n-type polycrystalline silicon is formed selectively. Further, in the pMODFET, a p-type source 15 and an n-type drain 16 are formed by selectively ion implanting a p-type dopant. In this case, formation of the

emitter region 34 by emitter annealing and activation of the source and drain can be applied in common (refer to FIG. 30(cg)).

Please replace page 39, first to third paragraphs of the Disclosure currently on file with the following three paragraphs:

Then, an insulation film 39 as a mask material for selective growth for the pMODFET is deposited over the entire surface and the insulation film 39, 26, 24, 23, and the field insulation film 2 are anisotropically etched in the region of the pMODFET. This is different from the Embodiment 6, since the source and the drain of the pMODFET are not connected with the electrodes in a self-aligned manner in this embodiment, an insulation film 7 comprising the silicon nitride film can be formed to the side wall of the opening of the insulation film. Accordingly, when a buffer layer 43 and a multi-layered film 44 comprising single-crystal silicon and single-crystal silicon-germanium are selectively grown epitaxially to the opening, generation of facets can be prevented (refer to FIG. 33(ad)).

After depositing a gate insulation film 50 and a gate electrode 51 and fabricating the gate electrode 51, an insulation film 47 is formed to the opening of the HBT and the side wall of the gate of the pMODFET (refer to FIG. 33(be)).

The insulation films 50 and 39 are removed by isotropic etching to expose the single-crystal silicon cap at the bottom of the opening of the HBT, and an emitter electrode 48 comprising a high concentration n-type polycrystalline silicon is formed selectively. Further, in the pMODFET, a p-type source 15 and p-type drain 16 are formed by ion implanting a p-type dopant selectively. In this case, formation of the emitter region 34 by emitter annealing and activation of the source-drain can be applied in common (refer to FIG. 33(cf)).